EXPEDITED PROCEDURE – EXAMINING GROUP 2116

S/N 09/964,010 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Matthew B. Haycock et al.	Examiner: Tse W. Chen
Serial No.:	09/964,010	Group Art Unit: 2116
Filed:	September 26, 2001	Docket No.: 884.455US1
Title:	METHOD AND APPARATUS FOR REALIGNING BITS ON A PARALLEL BUS	
Assignee:	Intel Corporation	Customer Number: 21186

AMENDMENT & RESPONSE UNDER 37 C.F.R. 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Final Office Action mailed July 29, 2005, please amend the application as follows:

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for responding to the Office action, thereby moving the deadline for response from October 29, 2005 to November 29, 2005.